REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed October 30, 2003. Claims 5, 6, 9, 12, 13, 15 - 19, and 22 have been cancelled in previous amendments without prejudice, waiver, or disclaimer. Claims 1 and 7 have been amended. The subject matter of amended claims 1 and 7 is contained within FIGs. 5 – 13 and the related detailed description of the specification. Consequently, no new matter has been added to the application. Upon entry of the amendments in this response, claims 1, 2, 4, 7, 8, 10, and 11 remain pending. Claims 1, 2, 4, 7, 8, 10, and 11 are patentable over the cited art of record. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Drawing Objections

The Office Action mailed May 28, 2003 (paper no. 7) objected to FIGs. 1 and 2A-2D. Applicant amended FIGs. 1 and 2A-2D to include the legend "prior art" via an amendment entered with an RCE. The Office Action mailed October 30, 2003 (paper no. 13) fails to address whether the objection to the drawings has been withdrawn. Unless Applicant is notified otherwise in a subsequent Office Action, Applicant assumes the previous amendment was responsive and the objection to the drawings withdrawn.

II. Claim Rejections Under 35 U.S.C. 112

A. Statement of the Rejection

The Office Action indicates that claims 1, 2, 4, 7, 8, 10, and 11 stand rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failure to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 7, the rejection alleges that the limitation "add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation in lines 13-15 is unclear whether the separate propagate, kill and generate bits are the bits of the result from the first carry-save adder or are another set of bits not from the first carry-save adder."

Concerning claims 2, 4, 8, 10, and 11, the rejection indicates that these dependent claims are allegedly unclear for the reason that they depend from claims 1 and 7.

B. Discussion of the Rejection

Applicant has amended independent claims 1 and 7 to more clearly point out and distinctly claim the subject matter of claims 1 and 7. Specifically, claim 1 recites, "a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder . . ." Thus, it is clear from lines 7-11 that the third propagate, kill, and generate recoded number representation is generated by the first carry-save adder. Thus, claim 1 is definite regarding the generation of the third propagate, kill, and generate recoded number (*i.e.*, it is generated within the first carry-save adder and does not comprise bits not from the first carry-save adder). Accordingly, the rejection of claim 1 and claims 2 and 4, which depend from claim 1, should be withdrawn.

Regarding claim 7, lines 5-7 of claim 7 clearly recite that a third propagate, kill, and generate recoded number is generated as a result of "adding a first propagate, kill, and generate recoded number and a second propagate, kill, and generate recoded number." Thus, claim 7 is definite regarding the origin of the third propagate, kill, and generate recoded number (*i.e.*, it is the result of adding the first and second propagate, kill, and generate recoded numbers). Accordingly, the rejection of claim 7 and claims 8, 10, and 11, which depend from claim 7, should be withdrawn.

III. Claim Rejections Under 35 U.S.C. 102

A. Statement of the Rejection

The Office Action indicates that claims 1, 2, 4, 7, 8, 10, and 11 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Bradley (U.S. Patent 6,496,846), hereafter *Bradley*.

B. Discussion of the Rejection

Applicant respectfully traverses the rejection of claims 1, 2, 4, 7, 8, 10, and 11 over *Bradley*. A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior-art reference disclose each element, feature, or step of the claim. See *e.g.*,

E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 7 USPQ2d 1129 (Fed. Cir. 1988). Applicant traverses the rejection of claims 1, 2, 4, 7, 8, 10, and 11 for at least the reason that *Bradley* fails to disclose, teach, or suggest each element and/or method step in the claims.

1. Claims 1, 2, and 4

Turning now to the specific claim rejections, claim 1 is exemplary. For convenience of analysis, independent claim 1, as amended, is repeated below in its entirety.

> 1. An apparatus for performing the addition of propagate, kill, and generate recoded numbers, said apparatus comprising:
>
> a ***circuitry configured to receive at least a first operand and a second operand, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations*** of respective first and second binary operands;
>
> ***a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation***; and
>
> a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation in accordance with a carry-in bit to generate a sum value and a carry value.

(Applicant's independent Claim 1 - *Emphasis added.*)

Applicant respectfully asserts that *Bradley* fails to disclose, teach, or suggest at least the emphasized elements as shown above. Consequently, claim 1 is allowable.

In this regard, *Bradley* apparently discloses a circuit and a method that encodes the carry-in bit as well as the operand bits for a binary addition of two streams of bits. (See Abstract and FIG. 1 of *Bradley*.) As apparently shown in FIG. 1, the circuit of *Bradley* includes an 8-bit encoder and a 8-bit adder that produce a first SUML and its compliment SUMH, as well as a 5-bit encoder and a 5-bit adder that produce a second SUML and its compliment SUMH. As apparently shown in *Bradley*, the 5-bit SUMH

and SUML results are concatenated to the 8-bit SUMH and SUML results. Significantly, *Bradley* fails to disclose, teach, or suggest adding two propagate, kill, and generate encoded operands to generate a third propagate, kill, and generate operand as recited in Applicant's claim 1.

In this regard, the Office alleges that encoding generator 105 including boxes 107-1, 108-1, and 109-1 teaches Applicant's first carry-save adder. Applicant disagrees. Applicant's claimed apparatus receives first and second operands "comprising respective first and second propagate, kill, and generate recoded number representations . . ." *Bradley* does not disclose, teach, or suggest an apparatus that receives first and second propagate, kill, and generate recoded number representations and generates a third propagate, kill, and generate recoded number. Applicant's claimed first carry-save adder receives the respective first and second propagate, kill, and generate recoded number representations and generates a third propagate, kill, and generate recoded number. *Bradley* does not disclose, teach, or suggest such an apparatus.

In contrast with Applicant's claimed apparatus, FIG. 1 and the related detailed description of *Bradley*, apparently illustrate and describe that encoding generator 105 is an eight-bit encoder that receives the first eight bits of thirteen-bit operands AH, AL, BH, and BL. *Bradley* does not disclose, teach, or suggest that operands AH, AL, BH, and BL are propagate, kill, and generate encoded operands. Consequently, *Bradley* does not disclose, teach, or suggest Applicant's claimed "***circuitry configured to receive at least a first operand and a second operand, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands***." For at least this reason, *Bradley* fails to anticipate claim 1. Thus, claim 1 is allowable and the rejection should be withdrawn.

Because *Bradley* fails to disclose, teach, or suggest Applicant's claimed circuitry configured to receive first and second propagate, kill, and generate recoded number representations, *Bradley* cannot disclose, teach, or suggest Applicant's claimed "***first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation***." For at least this additional reason, *Bradley* fails to anticipate claim 1. Thus, claim 1 is allowable and the rejection should be withdrawn.

Because *Bradley* fails to disclose, teach, or suggest Applicant's claimed ***third propagate, kill, and generate recoded number***, *Bradley* cannot disclose Applicant's claimed "***modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation in accordance with a carry-in bit to generate a sum value and a carry value***." For at least this additional reason, *Bradley* does not anticipate Applicant's claim 1 and is allowable.

Because independent claim 1 is allowable, as argued above, dependent claims 2 and 4 are also allowable. *See In re Fine,* 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, Applicant respectfully requests that the rejection of claims 1, 2, and 4 be withdrawn.

2. Claims 7, 8, 10, and 11

Claim 7 is also exemplary. For convenience of analysis, independent claim 7, as amended, is repeated below in its entirety.

> 7. A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:
> receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;
> ***adding the first and second propagate, kill, and generate representations to generate a third propagate, kill, and generate representation***; and
> ***mathematically combining the third propagate, kill, and generate representation in accordance with the carry-in value to generate a sum value and a carry value.***

(Applicant's independent Claim 7 - *Emphasis added.*)

Significantly, *Bradley* fails to disclose, teach, or suggest the step of "***adding the first and second propagate, kill, and generate representations to generate a third propagate, kill, and generate representation***" as recited in Applicant's claim 7. Consequently, *Bradley* does not disclose, teach, or suggest at least this step of Applicant's claim 7. For at least this reason, *Bradley* fails to anticipate claim 7. Thus, claim 7 is allowable and the rejection should be withdrawn.

Because *Bradley* fails to disclose, teach, or suggest a third propagate, kill, and generate recoded number representation generated via the addition of first and second propagate, kill, and generate recoded number representations, *Bradley* cannot disclose Applicant's claimed method step of "***mathematically combining the third propagate, kill, and generate representation and the carry-in value to generate a sum value and a carry value***." For at least this separate and independent reason, *Bradley* does not anticipate Applicant's claim 7.

Because independent claim 7 is allowable, as argued above, dependent claims 8, 10, and 11 are also allowable. *See In re Fine, supra.* Accordingly, Applicant respectfully requests that the rejection of claims 7, 8, 10, and 11 be withdrawn.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1, 2, 4, 7, 8, 10 , and 11 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby requested. If the Examiner believes that a telephone conference would expedite the prosecution of the application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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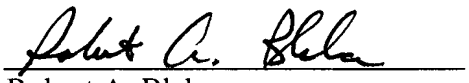
By: 

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